СИСТЕМА РАЗДЕЛЕНИЯ DSP-FPGA ДЛЯ БЕСПРОВОДНЫХ БАЗОВЫХ СТАНЦИЙ

DSP-FPGA SYSTEM PARTITIONING FOR WIRELESS BASE STATIONS

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While suppliers of digital signal processing (DSP) chips and programmable logic may differ over which device type is pre-eminent for new wireless system designs, what is important is what customers are actually implementing. Today, designers are applying a mix of both PLDs and DSP chips to meet market demand. The "intelligent partitioning" between these two device types gives wireless systems the best combination of features and cost-effectiveness. In addition to meeting the design specifications, applying a mix of DSP chips and FPGAs brings a measure of future proofing as well as potential for risk-free cost reduction. This article expands on these design strategies and provides examples of FPGA+DSP system partitioning for wireless base stations that illustrate why combining programmable logic with DSP can assist designers with their projects.

Introduction

Wireless operators are looking to increase their average revenue per user (ARPU) by offering enhanced data services, thus driving the need for higher bandwidth and consequently higher data rates. In addition, the need to offer the subscriber a rich user experience is transforming the underlying network architecture. Voice-centric technologies like narrowband 2G GSM, IS-95 systems have evolved to current-generation WCDMA-based HSDPA and HSUPA systems supporting peak data rates up to 10 Mbps. For future 3GPP long-term evolution specifications, complex signal processing techniques such as multiple-input multiple-output (MIMO), along with new radio technologies like orthogonal frequency-division multiple access (OFDMA) and multicarrier Code Division Multiple Access (MC-CDMA), are considered key to achieving target throughputs in excess of 100 Mbps. Alternate OFDM-based broadband wireless systems such as WiMAX have similarly evolved, achieving transmission speeds in excess of 70 Mbps.

The improvement in data rates has been possible primarily through the use of higher order modulation techniques and variable rate channel coding, commonly referred to as adaptive modulation and coding (AMC). Complex spatial signal processing schemes, such as beam forming and MIMO antenna techniques, are also proven technologies for increasing data rates at the expense of additional computational complexity. These enabling technologies pose significant challenges for OEMs needing to design base stations that are not only scalable and cost-effective but also flexible and reusable across multiple evolving standards.

Base station Design Requirements

Wireless systems designers need to meet a number of critical requirements including processing speed, flexibility, and time-to-market, all of which ultimately drive the hardware platform choice.

Processing Bandwidth

WiMAX and LTE broadband wireless systems have significantly higher throughput and data rate requirements than W-CDMA and cdma2000 cellular systems. To support these high data rates, the underlying hardware platform must have significant processing bandwidth. In addition, advanced signal processing techniques such as Turbo coding/decoding, and front-end functions including fast Fourier transform/inverse fast Fourier transform (FFT/IFFT), beam forming, MIMO, crest factor reduction (CFR), and digital predistortion (DPD) are computationally intensive and require several billion multiply and accumulate (MAC) operations per second.

WiMAX is a relatively new market and is currently in the initial development and deployment stages. Similarly, 3GPP LTE is being defined and will go through numerous revisions before being finalized. While there are many competing mobile broadband technologies, such as WiMAX, LTE, and UMB, their

common thread is OFDMA-MIMO. In this current scenario, having a flexible and reprogrammable product is necessary to provide a standards-agnostic or multi-protocol base station. Systems offering this flexibility can significantly reduce the capital
Expenditures and operating expenditures for wireless infrastructure OEMs and operators while alleviating risks posed by constantly evolving standards.

Cost-Reduction Path

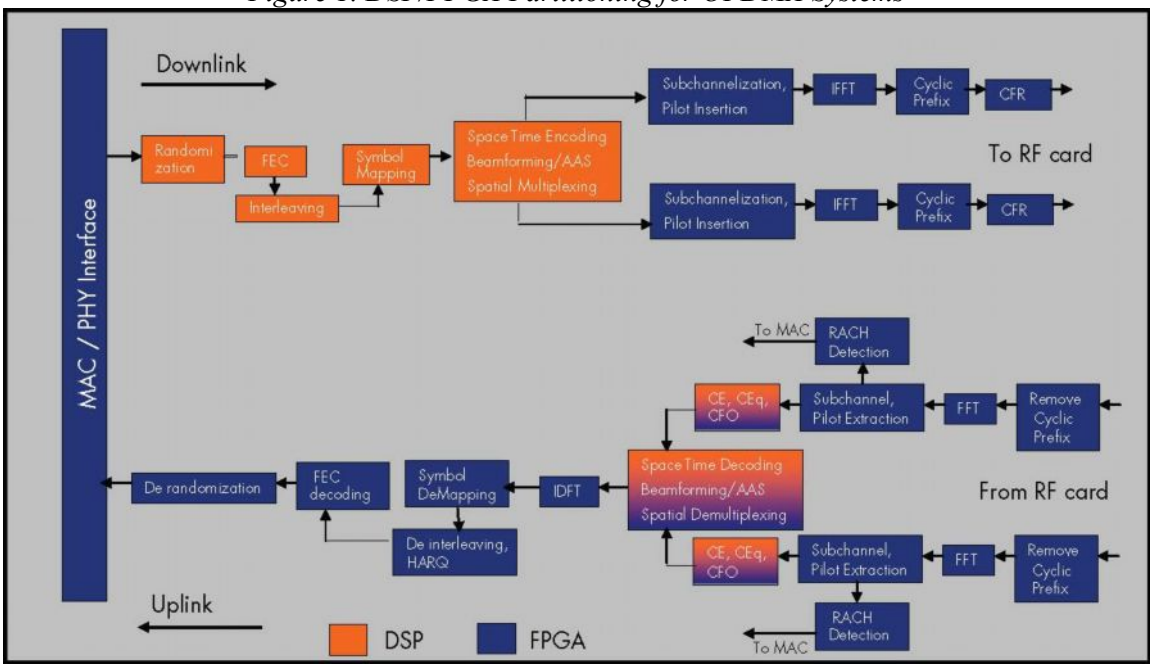
A valuable lesson learned from designing and deploying 3G systems is the importance of establishing a long-term cost-reduction strategy in the beginning. Evolving WiMAX and LTE standards are expected to stabilize. For OEMs and service providers to remain competitive in the marketplace, the cost of the final product eventually will be more important than flexibility. Choosing the right hardware platform also provides a seamless cost-reduction path for production volumes, saving millions of dollars in engineering costs that would otherwise be incurred by system redesign.

System Architecture Design and Logic Task Partitioning

Signal-processing data path and control operations make up the bulk of the processing load in a wireless basestation. Most architectures implement the system control, configuration, and the signal-processing data path using a combination of microcontrollers (MCUs), FPGAs, and programmable digital signal processors. The MCU controls the system, while the FPGA and digital signal processor handle the data-flow processing. Systems with light processing demands and control-oriented tasks are realized in software on a digital signal processor; heavier loads are best implemented in FPGAs that provide significant parallel processing benefits. The combination of digital signal processors and FPGAs ensures complete system flexibility and offers reprogrammability to fix bugs or even support entirely different standards.

The partitioning between FPGAs and digital signal processors depends on processing requirements; system bandwidth as well as system configuration; and the number of transmit and receive antennas. Figure 1 shows a typical digital signal processor/FPGA partitioning for baseband physical layer (PHY) functions in an OFDMA-based system such as WiMAX or LTE.

Figure 1. DSP/FPGA Partitioning for OFDMA Systems



By incorporating advanced multiple antenna technologies, the throughput offered by such systems is expected to be over 100 Mbps. The baseband PHY functionality can be broadly categorized into bit-level processing and symbol-level processing functions. The following section covers these functions and how FPGAs are used to complement DSP blocks for implementing both bit-level and symbol-level functions.

Bit-Level Processing

The bit-level blocks include randomization, forward error correction (FEC), interleaving, and mapping to

quadrature phase shift keying (QPSK) and quadrature amplitude modulation (QAM) functions on the transmit side. The corresponding receive processing bit-level blocks are symbol de-mapping, de-interleaving, FEC decoding, and de-randomization. Transmit bit-level functions are relatively straightforward and not computationally intensive. For example, randomization involves modulo-2 addition of the data bits with the output of a simple pseudo-random binary sequence generator. Although FPGAs offer more flexibility for bit-level manipulations than digital signal processors with fixed bus widths, the low computational complexity allows such functions to be implemented on digital signal processors easily. However, with growing throughput requirements, Turbo encoding could potentially be off-loaded to FPGAs to increase the system performance. On the receive side, FEC decoding-including Viterbi decoding, Turbo convolutional decoding, Turbo product decoding, and LDPC decoding-is computationally intensive and consumes significant bandwidth when implemented on digital signal processors.

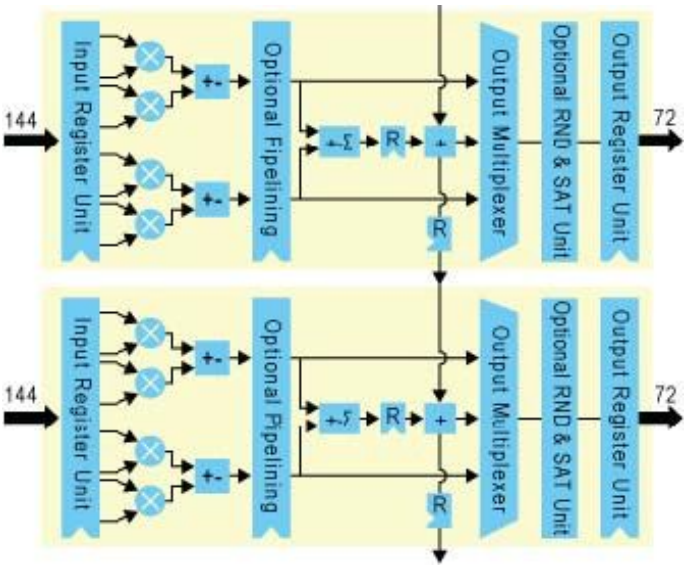
FPGAs are widely used to offload these functions and free up bandwidth on digital signal processors to perform other functions. Implementing other bit-level functions such as de-randomization, de-rate matching and hybrid ARQ on the same FPGA minimizes the data transfer between the FPGA and digital signal processor, leading to reduced latency and power consumption in the overall system. The same FPGA also can be used to interface to the MAC layer as well as implement certain lower MAC functions such as encryption/decryption and authentication.

Symbol-Level Processing

Symbol-level functions in OFDMA systems include functions such as sub-channelization and de-subchannelization, FFT/IFFT, channel estimation/equalization and ranging/random access channel (RACH) detection functions. Additional functions include DFT/IDFT (LTE specific), and potentially CFR if implemented on the channel card. Channel estimation and equalization can be performed offline and involve more control-oriented algorithms that are better suited for digital signal processors. Conversely, FFT/IFFT and DFT/IDFT functions are regular data path functions involving complex multiplications at very high speeds and are better suited for implementation on FPGAs. Functions such as RACH detection and CFR also require high-performance, low-latency FFT/IFFT.

Figure 2 shows the embedded DSP blocks contained in a high-end FPGA (Altera® Stratix® III device). DSP blocks usually have up to eight dedicated multipliers; however, an advanced FPGA like Stratix III EP3SE110 has 112 DSP blocks with 896 18 x 18 multipliers that offer a throughput of nearly 500 giga multiply-accumulate operations (GMACs). This is an order of magnitude higher than current off-the-shelf digital signal processors available in the market.

Figure 2. Embedded DSP Blocks Architecture in Stratix III FPGAs



The massive difference in signal processing capability between FPGAs and digital signal processors is further accentuated when dealing with basestations employing advanced multiple antenna techniques such as space time coding (STC), beamforming, and MIMO schemes. The combination of OFDM-MIMO is

widely regarded as a key enabler of higher data rates in current and future WiMAX and LTE wireless systems.

Figure 1 shows multiple transmit and receive antennas employed at a basestation. In this station, symbol processing functions are implemented separately for each antenna stream before MIMO decoding is performed, producing a single bit-level data stream. The symbol-level complexity grows linearly when the antennas implemented on digital signal processors perform operations in a serial manner. For example, when two transmit and two receive antennas are used, the FFT and IFFT functions consume approximately 60 percent of a 1-GHz digital signal processor, where the transform size is assumed to be 2048 points. In contrast, a multiple antenna-based implementation scales very efficiently when implemented with FPGAs. FPGAs provide parallel processing and time-multiplexing between the data from multiple antennas. The same 2x2-antenna FFT/IFFT configuration can be implemented using less than ten percent of a Stratix III EP3SE110 FPGA.

Multiple antenna schemes provide various benefits including higher data rates, array gain, diversity gain, and co-channel interference suppression. Beamforming and spatial multiplexing MIMO techniques are also computationally intensive, involving matrix decompositions and multiplications. Specifically, Cholesky decomposition, QR decomposition, and singular value decomposition functions are useful in solving the linear set of equations common in these systems. While these functions quickly exhaust DSP capabilities, they are well suited for FPGAs using well known systolic array architectures that provide a more cost-effective solution by exploiting FPGA parallelism.

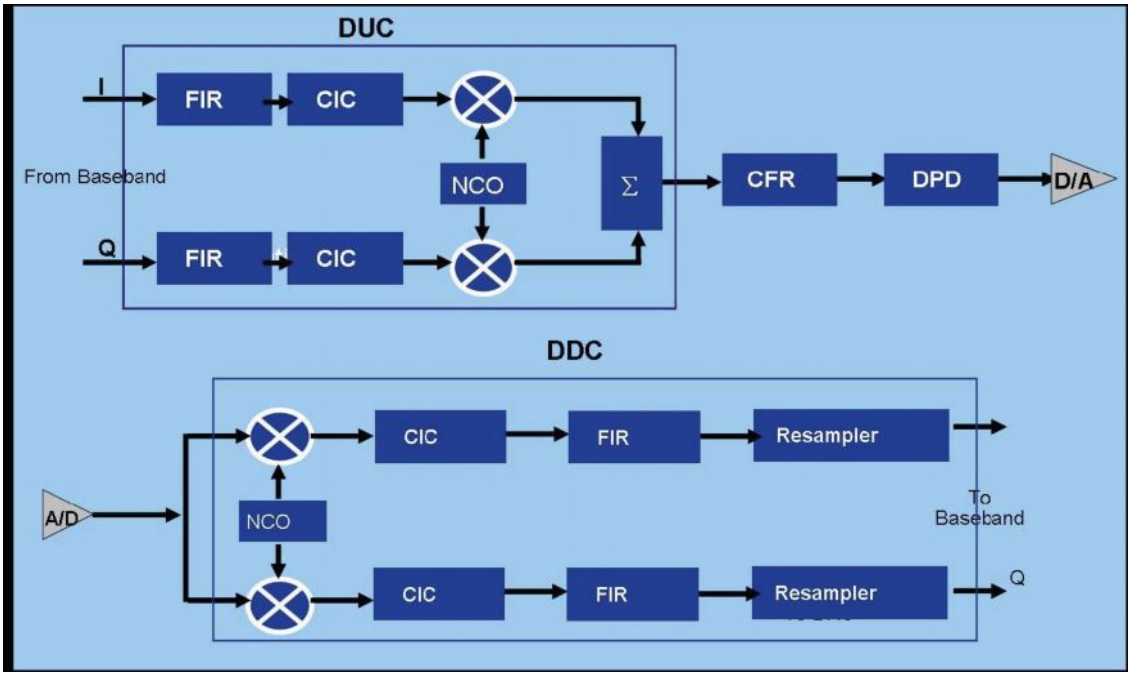
Digital IF Processing and RRHs

Figure 3 shows data from a baseband channel card sent to a RF card for subsequent digital intermediate frequency (IF) processing, including digital up conversion (DUC), CFR, and DPD. Digital IF extends the scope of digital signal processing beyond the baseband domain to the antenna-to the RF domain. This increases the flexibility of the system while reducing manufacturing costs. Moreover, digital frequency conversion provides greater flexibility and higher performance (in terms of attenuation and selectivity) than traditional analog techniques. CFR and DPD functions are required to improve the efficiency of power amplifiers used in base stations and consequently offer a significant OPEX savings. Both CFR and DPD involve complex multiplications at sample rates as high as 100+ MSPS. Similar to DUC, digital down conversion (DDC) is required on the receive side to bring the IF frequency down to baseband.

The introduction of MIMO and multi-carrier architectures calls for time-multiplexing and multi-channel implementations. Using Altera's IP cores and innovations in the DSP Builder tool, these tasks can easily be performed on an Altera FPGA. Both DUC and DDC use complex filter architectures including finite impulse response (FIR) and cascaded integrator-comb (CIC) filters. Advanced FPGAs provide hundreds of 18x18 multipliers running at speeds as high as 350 MHz. Not only does this provide a platform capable of processing multiple channels in parallel, it also yields a cost-effective, integrated single-chip solution.

Another trend is the concept of distributed BTS, where the radio unit is located remotely with respect to rest of the BTS instead of coexisting. These radio units, also called remote radio heads (RRHs), communicate with the main BTS unit over an optical link. CPRI and OBSAI are two standards that enable deploying RRHs. CPRI and OBSAI interfaces traditionally are implemented on FPGAs and the multichannel nature of this BTS architecture lends to a very cost-effective solution.

Figure 3. Digital IF Processing Functions



Conclusion

As standards stabilize, the initial need for flexibility in base stations should subside. At this stage, high performance and a long-term cost-reduction path become critical for market success. ASIC implementation has typically been the chosen cost-reduction route. Choosing FPGAs that have a risk-free migration path to low-cost ASIC-like technology will enable significant cost savings during the later stages of a product lifecycle. As an example, Altar's Hardcopy® II technology provides a seamless, risk free migration path from Stratix II FPGAs to a significantly lower cost ASIC-like solution, while also increasing system performance. Hardcopy products offer up to 70 percent cost reduction as well as lower power dissipation and smaller package, addressing both the CAPEX and OPEX components of the cost.

Concurrent application of digital signal processors and PLDs in wireless base station designs will continue as an effective design approach. What is essential to product success is intelligent partitioning of base station architectures derived from system throughput requirements and long-term cost considerations. This will ensure final products that are not only scalable and cost-effective, but flexible and reconfigurable across multiple evolving standards.

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